DETAILED ACTION

This second non-final action is in response to the amendment filed 09/18/2009. Claims 4,

16, & 27-33 are pending and have been considered as follows.

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

2.   Claims 4, 16, & 27-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Sugasawara (US-6043672-A) in view of Beasley et al. ("iDD pulse response testing applied to

complex CMOS ICs").

Claims 4 & 16:

Sugasawara discloses a fault analysis method of presuming a fault location of a semiconductor

IC and a fault analysis apparatus configured to presume a fault location of a semiconductor IC

comprising,

-       "applying a power supply voltage to said semiconductor IC" (i.e. "A selectable power

        supply line for providing power to a particular section of the integrated circuit is activated

        by an enable signal provided to a selectable power supply switch coupled to the

        selectable power supply line") [column 3 lines 28-32];

- "supplying a test pattern sequence having a plurality of test patterns to said
  semiconductor IC" (i.e. "Test development strategies include functional test wherein
  automatic test equipment (ATE) test programs are performed in which the circuit under
  test is stimulated with specified inputs while the outputs are monitored to determine if
  they correspond with simulated logic values") [column 1 lines 54-58];

- "the electrical potentials at the one or more locations are expected to change once the test
  pattern sequence is supplied" (i.e. "Defects in integrated circuits take many forms, some
  of which are test pattern sensitive…Quiescent current tests differ in that current is sensed
  rather than voltage, providing a simple means to monitor the entire circuit or portions
  thereof for over-current conditions") [column 1 lines 64-65 & column 2 lines 25-28];

- "measuring a time integral of a transient power supply current generated on said
  semiconductor IC in accordance with the change of said test pattern" (i.e. "Once halted
  (i.e., no transistor state switching is occurring) the power supply of the device under test
  is measured by the ATE and the resulting value is compared to predetermined reference
  values or test limits") [column 2 lines 14-18];

- "determining whether said transient current shows abnormality or not" (i.e. "the device
  under test is measured by the ATE and the resulting value is compared to predetermined
  reference values or test limits. Such quiescent current tests are effective in detecting
  many faults that would otherwise not be found by other test strategies") [column 2 lines
  16-20];

- "presuming a fault location out of said fault location list based on said test pattern sequence" (i.e. "This approach has typically included measuring current in a region of the integrated circuit, cutting lines to sections within the same region other than the section of interest, and then taking a additional measurements of current in the region") [column 2 lines 49-53];

- "the transient power supply current shows abnormality and said fault location list" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];

- "said transient power supply current is determined to be abnormal in a case that the time integral of said transient power supply current is over a predetermined value in said step of determining" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];

but, Sugasawara does not explicitly disclose,

- "storing a fault location list for the test pattern sequence," although Sugasawara does suggest an automated test equipment that would store test pattern sequences and which portions of the semiconductor integrated circuit have been isolated for testing, as recited below;

- "the fault location list includes one or more locations of components in said IC," although Sugasawara does suggest several components of a semiconductor integrated circuit that are tested for defects, as recited below;

- "said presuming comprises: deleting analysis points corresponding to the test pattern

   sequence where the transient power supply current does not show abnormality from

   analysis points corresponding to the test pattern sequence where the transient power

   supply current shows abnormality," although <u>Beasley et al.</u> do suggest determining which

   circuit tests result in a fault, as recited below;

- "presuming a remaining analysis point out of the analysis points corresponding to the test

   pattern sequence where the transient power supply current shows abnormality to be a

   fault location," although <u>Beasley et al.</u> do suggest determining which circuits are

   defective based on the completed fault tests, as recited below;

however, <u>Sugasawara</u> does disclose,

- "automated test equipment (ATE)" [column 5 line 11];

- "CMOS circuits use complementary p-channel metal-oxide-semiconductor field-effect

   (PMOS) transistors and n-channel metal-oxide-semiconductor field-effect (NMOS)

   transistors... Gate oxide defects, drain to source current leaks (punch-through), and p-n

   junction current leaks (such as drain or source to diffusion current leaks)" [column 1 lines

   36-39, 66-67 & column 2 line 1];

whereas, <u>Beasley et al.</u> do disclose,

- "...Table 2 SME scoring of the iDDPRT Time-Domain Tests for the SA3865. The time-

   domain tests performed up to this point for the SA3865 show limited success for

   detecting functional failures. While the success rate (85.7%) is promising, it is not

   satisfactory for full device screening in a manufacturing environment. Four functional

   failures were misclassified as "Good." On the other hand, 11 of the 15 functional failures

were successfully removed from the test lot without requiring additional expensive test

time. The time-domain tests for the SA3865 provided the following useful results: the

iDDPRT test shows good promise for detecting functional failures...the iDDPRT time

domain analysis technique used in this test was not suitable for detecting IDDQ

failures...Since this analysis is described by a simple equation, and can be performed

rapidly, it has the potential to be implemented in a production test program..." [page 34];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "storing a fault location list for the test pattern sequence" and

"the fault location list includes one or more locations of components in said IC" and "said

presuming comprises: deleting analysis points corresponding to the test pattern sequence where

the transient power supply current does not show abnormality from analysis points

corresponding to the test pattern sequence where the transient power supply current shows

abnormality" and "presuming a remaining analysis point out of the analysis points corresponding

to the test pattern sequence where the transient power supply current shows abnormality to be a

fault location," in the invention as disclosed by Sugasawara since predetermined reference values

or test limits would typically be stored within the testing device in order to be compared to the

resulting value(s) and for the purposes of determining which circuits are defective/faulty using

the processing of elimination as would be obvious to one of ordinary skill in the art.

Claim 27:

<u>Sugasawara</u> discloses a fault analysis apparatus configured to presume a fault location of

semiconductor IC comprising,

- "a power supply configured to apply a power supply voltage to said semiconductor IC"

    (i.e. "A selectable power supply line for providing power to a particular section of the

    integrated circuit is activated by an enable signal provided to a selectable power supply

    switch coupled to the selectable power supply line") [column 3 lines 28-32];

- "a test pattern sequence input unit configured to supply a test pattern sequence

    comprising a plurality of test patterns to said semiconductor IC" (i.e. "Test development

    strategies include functional test wherein automatic test equipment (ATE) test programs

    are performed in which the circuit under test is stimulated with specified inputs while the

    outputs are monitored to determine if they correspond with simulated logic values")

    [column 1 lines 54-58];

- "the electric potentials at the one or more locations are expected to change once the test

    pattern sequence is supplied" (i.e. "Defects in integrated circuits take many forms, some

    of which are test pattern sensitive…Quiescent current tests differ in that current is sensed

    rather than voltage, providing a simple means to monitor the entire circuit or portions

    thereof for over-current conditions") [column 1 lines 64-65 & column 2 lines 25-28];

- "an integral transient power supply current measuring unit configured to measure a time

    integral of a transient power supply current generated on said semiconductor IC in

    accordance with the change of said test pattern" (i.e. "Once halted (i.e., no transistor state

switching is occurring) the power supply of the device under test is measured by the ATE

and the resulting value is compared to predetermined reference values or test limits")

[column 2 lines 14-18];

- "a fault detector configured to determine that said transient power supply current is

   abnormal in a case that the time integral of said transient power supply current is over a

   predetermined value" (i.e. "the device under test is measured by the ATE and the

   resulting value is compared to predetermined reference values or test limits. Such

   quiescent current tests are effective in detecting many faults that would otherwise not be

   found by other test strategies") [column 2 lines 16-20];

- "a fault location presuming unit configured to presume a fault location out of said fault

   location list based on said test pattern sequence" (i.e. "This approach has typically

   included measuring current in a region of the integrated circuit, cutting lines to sections

   within the same region other than the section of interest, and then taking a additional

   measurements of current in the region") [column 2 lines 49-53];

- "the transient power supply current shows abnormality and said fault location list" (i.e.

   "In order to isolate the defective area of an integrated circuit, a failure analysis engineer

   seeks to determine which section of the integrated circuit is responsible for unusual

   current levels") [column 2 lines 38-41];

but, Sugasawara does not explicitly disclose,

- "a fault location list memory unit configured to store a fault location list for the test
  pattern sequence," although Sugasawara does suggest an automated test equipment that
  would store test pattern sequences and which portions of the semiconductor integrated
  circuit have been isolated for testing, as recited below;

- "the fault location list includes one or more locations of components in said IC," although
  Sugasawara does suggest several components of a semiconductor integrated circuit that
  are tested for defects, as recited below;

- "said fault location presuming unit is configured to presume the fault location by:
  deleting analysis points corresponding to the test pattern sequence where the transient
  power supply current does not show abnormality from analysis points corresponding to
  the test pattern sequence where the transient power supply current shows abnormality,"
  although Beasley et al. do suggest determining which circuit tests result in a fault, as
  recited below;

- "presuming a remaining analysis point out of the analysis points corresponding to the test
  pattern sequence where the transient power supply current shows abnormality to be a
  fault location," although Beasley et al. do suggest determining which circuits are
  defective based on the completed fault tests,, as recited below;

however, <u>Sugasawara</u> does disclose,

- "automated test equipment (ATE)" [column 5 line 11];

- "CMOS circuits use complementary p-channel metal-oxide-semiconductor field-effect
  (PMOS) transistors and n-channel metal-oxide-semiconductor field-effect (NMOS)
  transistors… Gate oxide defects, drain to source current leaks (punch-through), and p-n
  junction current leaks (such as drain or source to diffusion current leaks)" [column 1 lines
  36-39, 66-67 & column 2 line 1];

whereas, <u>Beasley et al.</u> do disclose,

- "…Table 2 SME scoring of the iDDPRT Time-Domain Tests for the SA3865. The time-
  domain tests performed up to this point for the SA3865 show limited success for
  detecting functional failures. While the success rate (85.7%) is promising, it is not
  satisfactory for full device screening in a manufacturing environment. Four functional
  failures were misclassified as "Good." On the other hand, 11 of the 15 functional failures
  were successfully removed from the test lot without requiring additional expensive test
  time. The time-domain tests for the SA3865 provided the following useful results: the
  iDDPRT test shows good promise for detecting functional failures…the iDDPRT time
  domain analysis technique used in this test was not suitable for detecting IDDQ
  failures…Since this analysis is described by a simple equation, and can be performed
  rapidly, it has the potential to be implemented in a production test program…" [page 34];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the

applicant's invention to include, "a means for storing a fault location list for the test pattern

sequence" and "a fault location list memory unit configured to store a fault location list for the

test pattern sequence" and "said fault location presuming unit is configured to presume the fault

location by: deleting analysis points corresponding to the test pattern sequence where the

transient power supply current does not show abnormality from analysis points corresponding to

the test pattern sequence where the transient power supply current shows abnormality" and

"presuming a remaining analysis point out of the analysis points corresponding to the test pattern

sequence where the transient power supply current shows abnormality to be a fault location," in

the invention as disclosed by Sugasawara since predetermined reference values or test limits

would typically be stored within the testing device in order to be compared to the resulting

value(s) and for the purposes of which circuits are defective/faulty using the processing of

elimination as would be obvious to one of ordinary skill in the art.

Claims 28-30:

Sugasawara and Beasley et al. disclose a fault analysis method of presuming a fault location of a

semiconductor IC, a fault analysis apparatus configured to presume a fault location of a

semiconductor IC, and a fault analysis apparatus configured to presume a fault location of

semiconductor IC, as in Claims 4, 16, & 27 above, their combination further comprising,

-    "the semiconductor IC is a CMOS IC" (i.e. "…CMOS ICs…") [Beasley et al. page 32].

Claims 31-33:

Sugasawara and Beasley et al. disclose a fault analysis method of presuming a fault location of a

semiconductor IC, a fault analysis apparatus configured to presume a fault location of a

semiconductor IC, and a fault analysis apparatus configured to presume a fault location of

semiconductor IC, as in Claims 28-30 above, their combination further comprising,

- "the time integral of said transient power supply current is a sum of integrals of transient

  currents that flow in logic gates of the CMOS IC" (i.e. "…The observed (oi) iDDPRT

  generated power-on transient current for each of the ICs in the SA3865 test lot were then

  compared to the expected (q) power-on transient current response using Eq. 1…") [page

  33].

Response to Arguments

3.   Applicant's arguments, see page 2, filed 09/18/2009, with respect to the rejection(s) of

claim(s) 4, 16, & 27-33 under 35 U.S.C. 103(a) have been fully considered and are persuasive.

Therefore, the rejection has been withdrawn. However, upon further consideration, a new

ground(s) of rejection is made in view of previously applied prior art in view of newly found

prior art.

Conclusion

4.   The prior art made of record and not relied upon is considered pertinent to the applicant's

disclosure.

        a.   <u>Beasley et al.</u> (US-5483170) - integrated circuit fault testing implementing

        voltage supply rail pulsing and corresponding instantaneous current response analysis;

        b.   <u>Sachdev et al.</u> ("Defect detection with transient current testing and its potential for

        deep submicron CMOS ICs");

5.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684.

The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for

Formal or Official faxes to Technology Center 2400 is 571-273-8300.

        Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private

PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you

would like assistance from a USPTO Customer Service Representative or access to the

automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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01/07/2010

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